

**REMARKS**

Claims 1 - 8 are pending in the present application. Reconsideration in view of the following remarks is respectfully requested. Applicant respectfully submits that this response is fully responsive to the Office Action dated **March 23, 2005**.

**Examiner Interview:**

The courtesies extended by Examiner Whipkey and Primary Examiner Moe to Applicant's representative, Tom Brown, during the June 2, 2005 Examiner Interview are gratefully appreciated. The substance of such interview is incorporated into the following remarks.

**Allowable Claim Subject Matter:**

Applicant gratefully acknowledges the indication in item 6 of the Office Action that claims 5, 7 and 8 are allowable.

Applicant also gratefully acknowledges the indication in item 5 of the Office Action that claim 4 would be allowable, if amended, to include all of the limitations of the base claim and any intervening claims. However, for at least the reasons stated below, it is respectfully submitted that all of claims 1 – 4 and 6 are allowable.

**As to the Merits:**

As to the merits of this case, the Examiner maintains the following rejections:

claims 1-3 stand rejected under 35 USC 103(a) as being unpatentable over Josephson (U.S. Patent No. 4,608,625, of record) in view of Ibori (U.S. Patent No. 5,465,202, of record);  
and

claim 6 stands rejected under 35 USC 103(a) as being unpatentable over Sawanobori in view of Ibori and Takeda.

Each of these rejections is respectfully traversed.

Claim 1 calls for *a first circuit for generating a positive polarity voltage, said first circuit including a rectifying circuit and a capacitor; a positive polarity voltage outputting terminal for outputting the positive polarity voltage from said first circuit; a second circuit for generating a negative polarity voltage; a negative polarity voltage outputting terminal for outputting the negative polarity voltage from said second circuit; a ground terminal for providing a reference potential for both of said positive polarity voltage and said negative polarity voltage; and a short circuit for short-circuiting substantially between said positive polarity voltage outputting terminal and said negative*

*polarity voltage outputting terminal in response to a power-off signal provided by the control circuit.*

During the interview, it was explained, for example, that in the present invention the power supply circuit includes a first circuit (24) for generating a positive polarity voltage and a positive polarity voltage outputting terminal (24a) for outputting the positive polarity voltage. It was further explained that the power supply circuit also include a second circuit (26) for generating a negative polarity voltage and a negative polarity voltage outputting terminal for outputting the negative polarity voltage (26a).

That is, it was pointed out that the positive polarity voltage of the output terminal (24a) and negative polarity voltage of the output terminal (26a) are each with respect to a ground terminal, for example, as shown in Fig. 1 of the present invention, which provides a reference potential for both of the positive polarity voltage and the negative polarity voltage.

Further, it was explained that in the present invention, for example, a short circuit (28) is used for short-circuiting between the positive polarity voltage outputting terminal (24a) and the negative polarity voltage outputting terminal (26a) in response to a power-off signal provided by a control circuit (18).

In contrast, while Ibori does disclose a d.c. intermediate circuit having a smoothing capacitor 3 which is discharged when the semiconductor switch 11 is turned on, the d.c. intermediate circuit does not include a negative polarity voltage outputting terminal for outputting the negative polarity voltage from a second circuit.

That is, Ibori fails to provide a ground terminal for providing a reference potential for both a positive polarity voltage and a negative polarity voltage.

More specifically, while Ibori may disclose a positive potential  $V_{pn}$  of the d.c. intermediate circuit (col. 3, lines 59-65), Ibori clearly fails to disclose a negative polarity voltage outputting terminal with respect to a ground terminal.

In other words, the semiconductor switch element 11 of Ibori short-circuits the line P and the line N which are included in a single circuit.

Moreover, it was also pointed out that the P and N shown in Fig. 1 merely represent a positive pole P and a negative pole N of the smoothing capacitor 3 (col. 1, lines 41-49), and not positive and negative voltage potentials.

As such, it is respectfully submitted that the applied references, singly or in combination, fail to disclose or fairly suggest the features of the present claimed invention concerning a *negative polarity voltage outputting terminal for outputting the negative polarity voltage from*

*said second circuit; a ground terminal for providing a reference potential for both of said positive polarity voltage and said negative polarity voltage; and a short circuit for short-circuiting substantially between said positive polarity voltage outputting terminal and said negative polarity voltage outputting terminal in response to a power-off signal provided by the control circuit.*

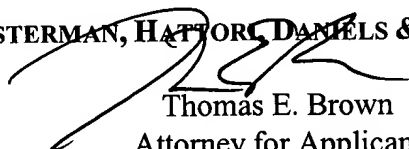
In view of the aforementioned remarks, Applicant submits that that the claims, as herein amended, are in condition for allowance. Applicant requests such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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